IN THE DRAWINGS

Applicants enclose a Replacement Sheet for Fig. 9. Please add the caption "Prior Art" to Fig. 9.

REMARKS

Claims 1-9 are pending in the application. Applicants amend claims 1, 6, and 9 for clarification, and refer to Fig. 1, its corresponding description, and page 20, lines 12-41 in the specification for exemplary embodiments of and support for the claimed invention. No new matter has been added.

The Examiner objected to Fig. 9 in the drawings under MPEP § 608.02(g) for failing to designate that which is old as "Prior Art." Applicants enclose a replacement sheet for Fig. 9 with the designation "Prior Art." Applicants respectfully request that the Examiner withdraw the objection.

The Examiner objected to claims 1 and 9 for a number of apparent informalities. Applicants amend claims 1 and 9 in accordance with the Examiner's suggestions, and respectfully request that the Examiner withdraw the objection.

Claims 1-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Admitted Prior Art ("AAPA") in view of U.S. Patent No. 6,662,216 to Lin. Applicants amend claims 1, 6, and 9 in a good faith effort to clarify the invention as distinguished from the cited references. Applicants respectfully traverse the rejection.

The Examiner asserted that AAPA discloses all aspects of the claimed invention except for the functions of the claimed access controller of each processor. The Examiner relied upon Lin as a combining reference that allegedly teaches these features.

Lin describes a technique for providing bus snooping capabilities to bus systems that do not inherently support such capabilities. In particular, Lin describes bus snooping in a multiprocessor system in which a plurality of master devices 208-212, such as CPUs, and a plurality of slave devices 214-216, such as common memories, are connected to a system bus

202, as illustrated in Fig. 4 of Lin. Each cache memory 242, 122 of each master device 208-212 stores part of data that are stored in the common memory 214-216. When a prescribed master device, such as a master device 210, writes data in the common memory 214, bus snooping units of other master devices 208-212 monitor a write command and address that flows on the system bus 202, and compare the address monitored on the system bus with the data addresses of their own cache memories. If there is a match in the address comparisons, the data stored in the matched addresses of each cache memory is invalidated. Thereafter, if the other master devices 208-212 need the latest data, they read it from the common memory 214 and stored it in their own cache memory as part of data that is stored in the common memory.

Thus, Lin describes each master device monitoring write commands and addresses that flow on the system bus. And when the data stored in the common memory is changed by a write command, the data stored in the cache memories of said each master device is invalidated. In other words, Lin only describes bus snooping for determining whether and when to invalidate "stale" cached data.

Lin, therefore, does not disclose an access controller of a processor that does not have access privilege accepting data written to the common memory and data read from the common memory, and storing this data in the storage unit within its own processor. Furthermore, neither AAPA nor Lin discloses each processor having a storage unit that stores same data and same control information as those stored in the common memory.

Thus, even assuming, arguendo, that it would have been obvious to one skilled in the art at the time the claimed invention was made to combine AAPA and Lin, the combination would still have failed to disclose or suggest,

> "[a] multiprocessor system comprising a common memory and a number of processors connected via a common bus, only one processor being allowed to access same data area of said common memory at a time, wherein:
>
> said common memory is provided with a number of data areas that store data and with a control information area that stores control information indicating whether each of the data areas is in use;
>
> each processor is provided with a storage unit for storing same data and same control information as those stored in the common memory and with an access controller; and
>
> the access controller of a processor that does not have access privilege monitors data and addresses that flow on the common bus, accepts data written to said common memory and data read from said common memory and stores this data in the storage unit within its own processor," as recited in claim 1. (Emphasis added)

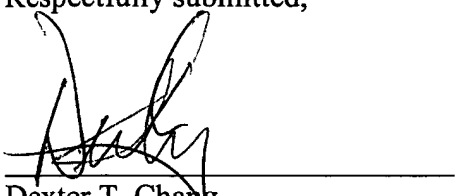
Accordingly, Applicants respectfully submit that claim 1, together with claims 2-5 dependent therefrom, is patentable over the cited references for at least the foregoing reasons. Claims 6 and 9 incorporate features that correspond to those of claim 1 cited above, and are, therefore, together with claims 7-8 dependent from claim 6, patentable over the cited references for at least the same reasons.

The above statements on the disclosure in the cited references represent the present opinions of the undersigned attorney. The Examiner is respectfully requested to specifically indicate those portions of the respective reference that provide the basis for a view contrary to any of the above-stated opinions.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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